CLAIMS

What is claimed is:

1. A circuit for tracking error signal detection on an optical storage medium, the optical storage medium detecting the reflective beams form which through a plurality of photo detectors to generate a plurality of signals, thereby generating a first summing signal and a second summing signal in order to obtain a tracking error signal, the circuit comprising:

a plurality of digitizers, for outputting the first summing signal and the second summing signal as a first digital summing signal and a second summing signal respectively, and outputting a third digital summing signal according to a third summing signal which is generated according to the first summing signal and the second summing signal;

a delayer for generating a delay signal according to the third digital summing signal; and

a plurality logic of comparators for outputting a first comparing signal after comparing the delay signal and the first digital summing signal, and a second comparing signal after comparing the delay signal and the second digital summing signal such that the tracking error signal is generated according to the first comparing signal and the second comparing signal.

2. The circuit of claim 1, wherein the digitizers further comprises a plurality of AC coupling capacitors, a plurality of registers and a plurality of slicers for coupling the first summing signal and the second summing signal respectively thereby generating the first digital summing signal and the second digital summing signal.

3. The circuit of claim 1, wherein the logic comparators are EXOR logic gates.

4. The circuit of claim 1, wherein the logic comparators are AND logic gates.

5. A circuit for tracking error signal detection on an optical storage medium, the optical storage medium detecting the reflective beams form which through a plurality of photo detectors to generate a plurality of signals, thereby generating a first summing signal and a second summing signal in order to obtain a tracking error signal, which is characterized in that:

summing a first summing signal and a second summing signal on order to obtaining a third summing signal, which is digitized to obtain a delay signal , thereby obtaining the tracking error signal according to the delay signal, the first summing signal and the second summing signal.

6. A circuit for tracking error signal detection on an optical storage medium, the optical storage medium detecting the reflective beams form which through a plurality of photo detectors to generate a plurality of signals, thereby obtaining a tracking error signal, the plurality of signals comprising a first signal, a second signal, a third signal and a fourth signal, the circuit comprising:

a plurality of digitizers for outputting the first signal, the second signal, the third signal and the fourth signal as a first digital signal, a second digital signal, a third digital signal and a fourth digital signal respectively, and outputting a first digital summing signal and a second digital summing according to a first summing signal and a second summing signal respectively, wherein the first summing signal is generated according to the first signal and the second signal, the second summing is generated according to the third signal and the fourth signal;

a plurality of delayers for generating a first delay signal and a second delay signal according to the first digital summing signal and the second digital summing signal respectively; and

a plurality of logic comparators for comparing the first delay signal and the first

digital signal, the first delay signal and the second digital signal, the second delay signal and the third digital signal, the second delay signal and the fourth digital signal respectively thereby outputting a first comparing signal, a second comparing signal, a third comparing signal and a fourth comparing signal, such that the tracking error signal is generated according to the first comparing signal, the second comparing signal, the third comparing signal and the fourth comparing signal.

7. The circuit of claim 6, wherein the digitizers further comprises a plurality of AC coupling capacitors, a plurality of registers and a plurality slicers for coupling the first signal, the second signal, the third signal and the fourth signal respectively thereby generating the first digital signal, the second digital signal, the third digital signal and the fourth signal.

8. The circuit of claim 6, wherein the logic comparators are AND logic gates.

9. A circuit for tracking error signal detection on an optical storage medium, the optical storage medium detecting the reflective beams form which through a plurality of photo detectors to generate a plurality of signals, thereby obtaining a tracking error signal, the plurality of signals comprising a first signal, a second signal, a third signal and a fourth signal, the circuit comprising:

a plurality of digitizers for outputting the first signal, the second signal, the third signal and the fourth signal as a first digital signal, a second digital signal, a third signal and a fourth signal respectively, and outputting a digital summing signal according to a summing signal, wherein the summing signal is generated according to the first signal, the second signal, the third signal and the fourth signal;

a delayer for generating a delay signal according to the digital summing signal; and

a plurality of logic comparators for comparing the delay signal and the first digital signal, the delay signal and the second digital signal, the delay signal and the third digital

signal, the delay signal and the fourth digital signal respectively thereby outputting a first comparing signal, a second comparing signal, a third comparing signal and a fourth comparing signal, such that the tracking error signal is generated according to the first comparing signal, the second comparing signal, the third comparing signal and the fourth comparing signal.

10. The circuit of claim 9, wherein the digitizers further comprises a plurality of AC coupling capacitors, a plurality of registers and a plurality slicers for coupling the first signal, the second signal, the third signal and the fourth signal respectively thereby generating the first digital signal, the second digital signal, the third digital signal and the fourth signal.

11. The circuit of claim 9, wherein the logic comparators are AND logic gates.